In the Claims

1. (Previously Presented) A method of fabricating a semiconductor device, having one or more layers of materials deposited on a polysilicon layer, comprising:

forming one or more features on the semiconductor device, each of the one or more features having sidewalls;

selectively depositing a first spacer comprising silicon nitride or an amorphous silicon film only on the sidewalls of each of the one or more features; and

reoxidizing the semiconductor device.

2. (Previously Presented) The method of claim 1, wherein forming one or more features comprises selectively etching the one or more features having sidewalls, thereby exposing the one or more layers of materials.

3. (Original) The method of claim 2, wherein the polysilicon layer serves as an etch stop.

4. (Previously Presented) The method of claim 1, wherein selectively depositing a first spacer further comprises limiting a deposition time to be less than an incubation time.

5. (Previously Presented) The method of claim 1, wherein selectively depositing a first spacer further comprises selectively depositing a thin silicon nitride.

6. (Previously Presented) A method of fabricating a semiconductor device, having one or more layers of materials deposited on a polysilicon layer, comprising:

selectively etching the semiconductor device to form one or more features having sidewalls exposing the one or more layers of materials, wherein the polysilicon layer serves as an etch stop;

selectively depositing a first spacer comprising silicon nitride or an amorphous silicon film only on the sidewalls of each of the one or more features; and

reoxidizing the semiconductor device.

7. (Previously Presented) The method of claim 6, wherein selectively depositing a first spacer further comprises limiting a deposition time to be less than an incubation time.

8. (Previously Presented) The method of claim 6, wherein selectively depositing a first spacer further comprises selectively depositing a thin silicon nitride.

9. (Previously Presented) A method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, comprising:

forming an insulating layer on a semiconductor wafer;

forming a conductive layer over the insulating layer;

forming a gate by etching, using the insulating layer as an etch stop, wherein the gate has sidewalls exposing the conductive layer and some portion of the insulating layer;

selectively forming a first oxidation barrier comprising silicon nitride or an amorphous silicon film only on the sidewalls of the gate; and

reoxidizing the structure.

10. (Previously Presented) The method of claim 9, wherein selectively forming a first oxidation barrier comprises selectively depositing a thin silicon nitride on the gate without depositing any on the source and the drain regions.

11. (Previously Presented) A method of forming a structure for controlling current flow between a source and a drain region in a semiconductor device, wherein the semiconductor device is composed of a semiconductor layer, an insulating layer disposed over the semiconductor layer, and a conductive layer disposed over the insulating layer, the method comprising:

forming a gate having sidewalls exposing the conductive layer and some portion of the insulating layer;

depositing a thin silicon nitride on the gate;

avoiding depositing the thin silicon nitride on the insulating layer disposed above the

source and the drain region; and

reoxidizing the structure.

12. (Previously Presented) The method of claim 11, wherein avoiding depositing the thin silicon nitride on the source and the drain region comprises limiting a deposition time to be less than an incubation time.

13-22. (Canceled)

23. (Previously Presented) The method of claim 1, further comprising:

forming a layer of gate oxide on a semiconductor layer; and

wherein:

forming one or more features further comprises patterning one or more electrodes on the gate oxide, each electrode comprising polysilicon, a refractory metal, and a dielectric;

selectively depositing a first spacer further comprises depositing the first spacer on the sidewalls of each electrode, the first spacer extending to and terminating at a boundary between each electrode and the gate oxide;

reoxidizing the semiconductor device comprises forming a layer of reoxidation on the first spacer and the gate oxide by a polycide reoxidation; and

further comprising forming a smile effect with the layer of reoxidation at the boundary.

24. (Previously Presented) The method of claim 1, wherein forming one or more features further comprises patterning one or more electrodes of undoped silicon on a layer of gate oxide on a semiconductor layer.

25. (Previously Presented) The method of claim 1, wherein forming one or more features further comprises patterning one or more electrodes on a layer of gate oxide on a semiconductor layer, each electrode comprising polysilicon, tungsten silicide, and a dielectric.

26. (Previously Presented) The method of claim 1, wherein selectively depositing a first spacer further comprises depositing Si_3N_4 only on the sidewalls of each of the one or more features at a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

27. (Previously Presented) The method of claim 1, further comprising depositing a second spacer to set a lateral dimension of a source/drain diffusion in the semiconductor device.

28. (Currently Amended) The method of claim 6, further comprising:

forming a layer of gate oxide on a semiconductor layer; and

wherein:

selectively etching further comprises selectively etching the semiconductor device to form one or more electrodes on the gate oxide, each electrode comprising [[the]] polysilicon, a refractory metal, and a dielectric;

selectively depositing a first spacer further comprises depositing the first spacer on the sidewalls of each electrode, the first spacer extending to and terminating at a boundary between each electrode and the gate oxide;

reoxidizing the semiconductor device comprises forming a layer of reoxidation on the first spacer and the gate oxide by a polycide reoxidation; and

further comprising forming a smile effect with the layer of reoxidation at the boundary.

29. (Previously Presented) The method of claim 6, wherein selectively etching further comprises selectively etching the semiconductor device to form one or more electrodes on a layer of gate oxide on a semiconductor layer, each electrode comprising polysilicon, tungsten silicide, and a dielectric.

30. (Previously Presented) The method of claim 6, wherein selectively depositing a first spacer further comprises depositing Si_3N_4 only on the sidewalls of each of the one or more features at a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

31. (Previously Presented) The method of claim 6, further comprising depositing a second spacer to set a lateral dimension of a source/drain diffusion in the semiconductor device.

32. (Currently Amended) The method of claim 9, wherein:

forming an insulating layer comprises forming a layer of gate oxide on a semiconductor wafer;

forming a conductive layer comprises forming a layer of polysilicon over the gate oxide;

forming a gate further comprises forming the gate comprising [[the]] polysilicon, a refractory metal, and a dielectric;

selectively forming a first oxidation barrier further comprises depositing a first spacer on the sidewalls of the gate for a period of time less than an incubation period for the deposition on the gate oxide and to a thickness less than an incubation thickness for the deposition on the gate oxide, the first spacer extending to and terminating at a boundary between the gate and the gate oxide;

reoxidizing the structure comprises forming a layer of reoxidation on the first spacer and the gate oxide by a polycide reoxidation; and

further comprising forming a smile effect with the layer of reoxidation at the boundary.

33. (Previously Presented) The method of claim 9, wherein forming a conductive layer comprises forming a layer of undoped silicon.

34. (Previously Presented) The method of claim 9, wherein forming an insulating layer comprises forming a layer of gate oxide.

35. (Previously Presented) The method of claim 9, wherein forming a gate further comprises forming the gate comprising polysilicon, tungsten silicide, and a dielectric.

36. (Previously Presented) The method of claim 9, wherein selectively forming a first oxidation barrier further comprises depositing Si_3N_4 only on the sidewalls of the gate at a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

37. (Previously Presented) The method of claim 11, wherein:

forming a gate comprises forming a gate having sidewalls exposing the conductive layer comprising polysilicon, a refractory metal, and a dielectric and some portion of the insulating layer comprising gate oxide;

depositing a thin silicon nitride further comprises depositing the silicon nitride on the sidewalls of the gate for a period of time less than an incubation period for the deposition on the gate oxide and to a thickness less than an incubation thickness for the deposition on the gate oxide, the silicon nitride extending to and terminating at a boundary between the gate and the gate oxide;

reoxidizing the structure comprises forming a layer of reoxidation on the silicon nitride and the gate oxide by a polycide reoxidation; and

further comprising forming a smile effect with the layer of reoxidation at the boundary.

38. (Previously Presented) The method of claim 11, wherein forming a gate comprises forming a gate having sidewalls exposing the conductive layer comprising undoped silicon and some portion of the insulating layer comprising gate oxide.

39. (Previously Presented) The method of claim 11, wherein forming a gate comprises forming a gate having sidewalls exposing the conductive layer comprising polysilicon, tungsten silicide, and a dielectric and some portion of the insulating layer comprising gate oxide.

40. (Previously Presented) The method of claim 11, wherein depositing a thin silicon nitride further comprises depositing Si_3N_4 only on the gate at a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

41. (Previously Presented) A method of forming a semiconductor device comprising:

forming an oxide layer;

forming at least one feature over the oxide layer, the feature having a surface and being contiguous with the oxide layer at a boundary; and

forming a spacer comprising silicon nitride or an amorphous silicon film covering the surface of the feature and terminating at a location adjacent to the boundary wherein the spacer is not in contact with the oxide layer.

42. (Previously Presented) The method of claim 41, wherein:

forming an oxide layer comprises forming a layer of gate oxide on a semiconductor layer;

forming at least one feature further comprises patterning one or more electrodes on the gate oxide, each electrode comprising polysilicon, a refractory metal, and a dielectric between sidewalls, the surface comprising the sidewalls;

forming a spacer further comprises depositing the silicon nitride on the sidewalls of each electrode for a period of time less than an incubation period for the deposition on the gate oxide and to a thickness less than an incubation thickness for the deposition on the gate oxide; and

further comprising:

forming a layer of reoxidation on the spacer and the gate oxide by a polycide reoxidation; and

forming a smile effect with the layer of reoxidation at the boundary.

43. (Previously Presented) The method of claim 41, wherein forming at least one feature further comprises patterning one or more electrodes of undoped silicon on the oxide layer.

44. (Previously Presented) The method of claim 41, wherein forming at least one feature further comprises patterning one or more electrodes comprising polysilicon, tungsten silicide, and a dielectric between sidewalls on the oxide layer, the surface comprising the sidewalls.

45. (Previously Presented) The method of claim 41, wherein forming a spacer further comprises depositing Si_3N_4 on the surface of the feature at a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

46. (Previously Presented) The method of claim 41, further comprising depositing a second spacer to set a lateral dimension of a source/drain diffusion in the semiconductor device.

47. (Previously Presented) A method of forming an electronic device comprising:

forming a first layer of oxide;

forming a feature over the first layer of oxide, the feature having a surface; and

forming a spacer comprising silicon nitride or an amorphous silicon film only on a substantially vertical portion of the surface of the feature.

48. (Previously Presented) The method of claim 47, wherein:

forming a first layer of oxide comprises forming a layer of gate oxide on a semiconductor layer;

forming a feature further comprises patterning one or more electrodes on the gate oxide, each electrode comprising polysilicon, a refractory metal, and a dielectric between sidewalls, the surface comprising the sidewalls;

forming a spacer further comprises depositing the spacer on the sidewalls of each electrode for a period of time less than an incubation period for the deposition on the gate oxide and to a thickness less than an incubation thickness for the deposition on the gate oxide, the spacer extending to and terminating at a boundary between each electrode and the gate oxide; and

further comprising:

forming a layer of reoxidation on the spacer and the gate oxide by a polycide reoxidation; and

forming a smile effect with the layer of reoxidation at the boundary.

49. (Previously Presented) The method of claim 47, wherein forming a feature further comprises patterning one or more electrodes of undoped silicon on the first layer of oxide.

50. (Previously Presented) The method of claim 47, wherein forming a feature further comprises patterning one or more electrodes comprising polysilicon, tungsten silicide, and a dielectric between sidewalls on the first layer of oxide, the surface comprising the sidewalls.

51. (Previously Presented) The method of claim 47, wherein forming a spacer further comprises depositing Si_3N_4 only on the surface of the feature at a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

52. (Previously Presented) The method of claim 47, further comprising depositing a second spacer to set a lateral dimension of a source/drain diffusion in the electronic device.

53. (Previously Presented) A method of forming an electronic device comprising:

forming a first layer of oxide;

forming a feature over the first layer of oxide, the feature having a surface;

forming a spacer comprising silicon nitride or an amorphous silicon film only on the surface of the feature; and

forming a second layer of oxide on the spacer and the first layer of oxide, the second layer of oxide forming a gap at a boundary between the feature and the first layer of oxide.

54. (Previously Presented) The method of claim 53, wherein:

forming a first layer of oxide comprises forming a layer of gate oxide on a semiconductor layer;

forming a feature further comprises patterning one or more electrodes on the gate oxide, each electrode comprising polysilicon, a refractory metal, and a dielectric between sidewalls, the surface comprising the sidewalls;

forming a spacer further comprises depositing the spacer on the sidewalls of each

electrode for a period of time less than an incubation period for the deposition on the gate oxide and to a thickness less than an incubation thickness for the deposition on the gate oxide, the spacer extending to and terminating at a boundary between each electrode and the gate oxide; and

forming a second layer of oxide comprises forming a layer of reoxidation on the spacer and the gate oxide by a polycide reoxidation.

55. (Previously Presented) The method of claim 53, wherein forming a feature further comprises patterning one or more electrodes of undoped silicon on the first layer of oxide.

56. (Previously Presented) The method of claim 53, wherein forming a feature further comprises patterning one or more electrodes on the first layer of oxide, each electrode comprising polysilicon, tungsten silicide, and a dielectric between sidewalls, the surface comprising the sidewalls.

57. (Previously Presented) The method of claim 53, wherein forming a spacer further comprises depositing Si_3N_4 only on the surface of the feature at a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

58. (Previously Presented) The method of claim 53, further comprising depositing a second spacer to set a lateral dimension of a source/drain diffusion in the electronic device.

59. (Previously Presented) A method of forming an electronic device comprising:

forming a first layer of oxide;

forming an electrode on the first layer of oxide, the electrode having sidewalls; and

depositing a spacer comprising silicon nitride or an amorphous silicon film only on the sidewalls of the electrode, the spacer extending to and terminating adjacent to a boundary between the first layer of oxide and the sidewalls of the electrode.

60. (Previously Presented) The method of claim 59, wherein:

forming a first layer of oxide comprises forming a layer of gate oxide on a semiconductor layer;

forming an electrode further comprises patterning the electrode on the gate oxide, the electrode comprising polysilicon, a refractory metal, and a dielectric;

depositing a spacer further comprises depositing the spacer on the sidewalls of the electrode for a period of time less than an incubation period for the deposition on the gate oxide and to a thickness less than an incubation thickness for the deposition on the gate oxide; and

further comprising:

forming a layer of reoxidation on the spacer and the gate oxide by a polycide reoxidation; and

forming a smile effect with the layer of reoxidation at the boundary.

61. (Previously Presented) The method of claim 59, wherein forming an electrode further comprises patterning the electrode, the electrode comprising undoped silicon on the first layer of oxide.

62. (Previously Presented) The method of claim 59, wherein forming an electrode further comprises patterning the electrode, the electrode comprising polysilicon, tungsten silicide, and a dielectric on the first layer of oxide.

63. (Previously Presented) The method of claim 59, wherein depositing a spacer further comprises depositing Si_3N_4 only on the sidewalls of the electrode at a temperature of 680°C, a pressure of 80 milliTorrs, and a flow ratio of 6:1.

64. (Previously Presented) The method of claim 59, further comprising depositing a second spacer to set a lateral dimension of a source/drain diffusion in the electronic device.